IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A non-volatile semiconductor memory device comprising:

an array of electrically rewritable nonvolatile data storage memory cells each having a transistor structure with a control gate, the control gate of a selected memory cell presently selected to be applied an identical voltage during an ordinary read operation and a verify-read operation;

a reference current source circuit configured to generate a first reference current adaptable for use during ~~an~~ said ordinary read operation and a second reference current for use during ~~a~~ said verify-read operation for data status verification in one of writing and erasing events, said reference current source circuit including reference cells each having a transistor structure with a control gate, the control gate of a reference cell presently selected to be applied said identical voltage during said ordinary read operation and said verify-read operation; and

a sense amplifier configured to compare read currents of a selected memory cell as selected during said ordinary read operation and said verify-read operation with the first and second reference currents respectively to thereby perform data detection~~; and~~

~~a driver configured to apply an identical voltage to the control gate of the selected memory cell presently selected and to apply said identical voltage to the control gate of the reference cell presently selected during said ordinary read operation and said verify-read operation~~.

2. (Original) The device according to claim 1, wherein said reference current source circuit includes:

an ordinary read use reference current source configured to generate said first reference current;

a verify-read use reference current source configured to generate said second reference current; and

a switch circuit configured to selectively connect said ordinary read use reference current source and said verify-read use reference current source to said sense amplifier.

3. (Currently Amended) The device according to claim 2, wherein said ordinary read use reference current source and said verify-read use reference current source are formed of reference cells being substantially the same in structure as said memory cells and different from each other in gate threshold voltage~~, each said reference cell having its control gate with a read voltage identical to that of said memory cells~~.

4. (Original) The device according to claim 1, wherein each said memory cell performs storage of multiple-value data based on a cell current distribution upon application of said read voltage to the control gate thereof, and wherein said reference current source circuit includes:

a plurality of ordinary read use reference current sources switchably rendered operative in accordance with data to be read during said ordinary read operation;

a plurality of verify-read use reference current sources switchably operable in accordance with data to be verified during said verify-read operation; and

a switch circuit configured to select one from among said ordinary read use reference current sources and said verify-read use reference current sources and to connect a selected one to said sense amplifier.

5. (Currently Amended) The device according to claim 4, wherein said ordinary read use reference current source and said verify-read use reference current source are formed of reference cells being substantially the same in structure as said memory cells and different in gate threshold voltage~~, each said reference cell having its control gate with a read voltage identical to that of said memory cells~~.

6. (Original) The device according to claim 1, wherein each said memory cell performs multiple-value data storage based on a cell current distribution upon application of said read voltage to the control gate thereof, and wherein said reference current source circuit includes:

a reference current source configured to output a fiducial current; and

a division converter circuit configured to be operatively responsive to receipt of the output current of said reference current source for producing a plurality of ordinary read use reference currents and a plurality of verify-read use reference currents and for selecting either one therefrom for supplement to said sense amplifier.

7. (Currently Amended) The device according to claim 6, wherein said reference current source is formed of ~~a~~ said reference cell being substantially the same in structure to said memory cells ~~and having a control gate with a read voltage identical to that of said memory cells being given thereto~~.

8. (Original) The device according to claim 7, wherein said division converter circuit has:

a load PMOS transistor configured to supply a current to said reference cell;

a plurality of current source PMOS transistors making up a current mirror circuit together with the load PMOS transistor, for generating the ordinary read use and verify-read use reference currents;

a switch circuit configured to selectively activate outputs of said plurality of current source PMOS transistors;

an output NMOS transistor configured to convert an output current as selected by said switch circuit to a voltage and for outputting the voltage; and

a current source NMOS transistor having a gate for receipt of an output voltage of said output NMOS transistor and a drain as connected to a reference node of said sense amplifier.

9. (Original) The device according to claim 1, wherein each said memory cell performs multiple-value data storage based on a cell current distribution upon application of said read voltage to the control gate thereof, and wherein said reference current source circuit includes:

at least two reference current sources; and

a difference division converter circuit configured to generate, based on a difference between output currents of said two reference current sources, a plurality of ordinary read use reference currents and a plurality of verify-read use reference currents and to select either one therefrom for connection to said sense amplifier.

10. (Currently Amended) The device according to claim 9, wherein said two reference current sources comprise a first reference cell and a second reference cell being substantially the same in structure to said memory cells, both said first and second reference cells being one of said reference cells ~~and having control gates for receipt of an applied read~~

~~voltage identical to that of said memory cells~~, said second reference cell permitting flow of a current greater than that of said first reference cell.

11. (Original) The device according to claim 10, wherein said difference division converter circuit includes:

a first PMOS current mirror circuit configured to supply to said second reference cell a current corresponding to an output current of said first reference cell;

a first output NMOS transistor configured to convert a current of said first PMOS current mirror circuit to a voltage;

a load PMOS transistor configured to supply to said first reference cell a difference current of currents of the first and second reference cells;

a plurality of current source PMOS transistors making up a second PMOS current mirror circuit together with said load PMOS transistor, for generating said ordinary read use reference currents and said verify-read use reference currents;

a switch circuit configured to selectively activate outputs of said current source PMOS transistors;

a second output NMOS transistor configured to convert a current as selected by said switch circuit to a voltage and to output the voltage; and

a couple of current source NMOS transistors having gates for receipt of respective output voltages of the first and second output NMOS transistors and drains each connected to a reference node of said sense amplifier.

12. (Original) The device according to claim 1, further comprising, for enabling measurement of a cell current distribution of write or erase data of said memory cells:

a reference current source pad for permitting connection of a reference node of said sense amplifier to an external reference current source.

13. (Original) The device according to claim 1, further comprising:

a reference current source pad for permitting connection to an external reference current source to thereby enable measurement of a cell current distribution of write or erase data of said memory cells;

a reference current generator circuit configured to generate a plurality of different reference currents based on a current of said external reference current source and to select one from among the reference currents for connection to a reference node of said sense amplifier; and

an external control signal pad for control of the reference current generator circuit in response to a control signal as externally supplied thereto.

14. (Original) The device according to claim 1, further

comprising, for enabling measurement of a cell current distribution of write or erase data of said memory cells:

a reference use transistor having a drain connected to a reference node of said sense amplifier and a source coupled to ground; and

an external voltage source pad for permitting connection of a gate of the reference use transistor to an external reference voltage source.

15. (Currently Amended) A nonvolatile semiconductor memory device with a plurality of read operation modes, comprising:

a memory cell array with electrically reprogrammable nonvolatile data storage memory cells disposed therein, a selected memory cell in said memory cell array to be applied a same read voltage for common use in said plurality of read operation modes;

a reference current source circuit configured to generate a plurality of reference currents to be used in said plurality of read operation modes, said reference current source circuit including reference cells, a reference cell presently selected to be applied said same read voltage for common use in said plurality of read operation modes;

~~a driver configured to apply a same read voltage for common use in said plurality of read operation modes to a selected memory cell in said memory cell array and to a reference cell presently selected;~~ and

a sense amplifier configured to detect data through comparison of a read current of said selected memory cell to one selected from among said plurality of reference currents in accordance with a read operation mode.

16. (Original) The device according to claim 15, wherein said plurality of read operation modes include an ordinary read operation mode and a verify-read operation mode during data writing or erasing.

17. (Original) The device according to claim 16, wherein said memory cells store therein multi-value data due to a cell current distribution upon receipt of said read voltage.

18. (Original) The device according to claim 16, wherein said reference current source circuit includes:

an ordinary read use reference current source configured to produce a reference current to be used in said ordinary read operation mode;

a verify-read use reference current source configured to produce a reference current for use in said verify-read operation mode; and

a switch circuit for selectively connecting said ordinary read use reference current source and said verify-read use reference current source to said sense amplifier.

19. (Currently Amended) The device according to claim 18, wherein said ordinary read use reference current source and said verify-read use reference current source are formed of said reference cells respectively and wherein said reference cells are identical in structure to said memory cells and different in gate threshold value from each other~~, the same read voltage as that of said memory cells being given to each said reference cell~~.

20. (Original) The device according to claim 17, wherein said reference current source circuit includes:

a plurality of ordinary read use reference current sources switchably used in accordance with data to be read in the ordinary read mode;

a plurality of verify-read use reference current sources switchably used in accordance with data to be verified in the verify-read mode; and

a switch circuit configured to selecting one from said ordinary read use reference current sources and said verify-read use reference current sources for connection to said sense amplifier.

21. (Currently Amended) The device according to claim 20, wherein each said ordinary read use reference current source and each said verify-read use reference current source are respectively formed of reference cells being identical in structure to said memory

cells and different in gate threshold value~~, the same read voltage as that of said memory cells being given to said reference cells~~.

22. (Original) The device according to claim 17, wherein said reference current source circuit includes:

a reference current source configured to output a fiducial current; and

a division converter circuit configured to be operatively responsive to receipt of the output fiducial current of said reference current source for generating a plurality of ordinary read use reference currents and a plurality of verify-read use currents and to select either one therefrom for supplement to said sense amplifier.

23. (Currently Amended) The device according to claim 22, wherein said reference current source is formed of a reference cell identical to said memory cells ~~both~~ in structure ~~and in read voltage as given thereto~~.

24. (Original) The device according to claim 22, wherein said division converter circuit includes:

a load PMOS transistor configured to supply a current to said reference cell;

a plurality of current source PMOS transistors making up a current mirror circuit together with the load PMOS transistor, for generating the ordinary read use and verify-read use reference currents;

a switch circuit configured to selectively activate outputs of said plurality of current source PMOS transistors;

an output NMOS transistor configured to convert an output current as selected by said switch circuit to a voltage and for outputting the voltage; and

a current source NMOS transistor having a gate for receipt of an output voltage of said output NMOS transistor and a drain as connected to a reference node of said sense amplifier.

25. (Original) The device according to claim 17, wherein said reference current source circuit includes:

two reference current sources; and

a difference division converter circuit configured to generate, based on a difference between output currents of said two reference current sources, a plurality of ordinary read use reference currents and a plurality of verify-read use reference currents and to select either one therefrom for connection to said sense amplifier.

26. (Currently Amended) The device according to claim 25, wherein said two reference current sources comprise a first reference cell and a second reference cell being substantially the same as said memory cells in structure, ~~and in read voltage applied thereto,~~ both said first and second reference cells being one of said reference cells, said second reference cell permitting flow of a current greater than that of said first reference cell.

27. (Original) The device according to claim 25, wherein said difference division converter circuit includes:

a first PMOS current mirror circuit configured to supply to said second reference cell a current corresponding to an output current of said first reference cell;

a first output NMOS transistor configured to convert a current of said first PMOS current mirror circuit to a voltage;

a load PMOS transistor configured to supply to said first reference cell a difference current of currents of the first and second reference cells;

a plurality of current source PMOS transistors making up a second PMOS current mirror circuit together with said load PMOS transistor, for generating said ordinary read use reference current and verify-read use reference current;

a switch circuit configured to selectively activate outputs of said current source PMOS transistors;

a second output NMOS transistor configured to convert a current as selected by said switch circuit to a voltage and to output the voltage; and

a couple of current source NMOS transistors having gates for receipt of respective output voltages of the first and second output NMOS transistors and drains each connected to a reference node of said sense amplifier.